AMENDMENTS TO THE DRAWINGS

The replacement sheet for sheet 12/16 includes amendments to Figs. 13, 14 and 15 of the drawings. Namely, an insulating film 2 having an opening was added in each of Figs. 13, 14 and 15, consistent with that set forth in, for example, claims 5 and 7 as well as that described in the Specification. A more detailed supportive discussion directed thereto is provided in the responsive remarks.

REMARKS

Reconsideration and early allowance of the above-identified application, as currently amended, is respectfully requested.

A number of revisions were implemented in the Specification that is of a minor grammatical/editorial clarifying nature. Incidentally, the expression "conduction type" was revised to the expression "conductivity type", which conforms to the more readily used expression. Also, on page 3 of the Specification, a descriptive statement was interlineated regarding reference numeral 103 of Fig. 19 of the drawings. Fig. 19 relates to JP-A 09-283533, discussed on page 3 of the Background of the Invention section of the present Specification. This layer 103 refers to layer 63 in Fig. 6 of the referred to prior Japanese published document (see the English language abstract thereof). The descriptive statement directed to reference numeral 103 in Fig. 19 of the drawings was added in order to comply with the drawing requirement in which each reference character illustrated must be mentioned in the Specification, 37C.F.R. 1.84(p)(5). It is submitted, the insertion is strictly directed to a point of clarification and does not involve the submission of new matter, noting that the drawing figure relates to a known illustration found in JP-A 09-283533, which is of record in the Specification, and a copy was submitted in an Information Disclosure Statement with the original application papers.

The status of the claims is as noted hereinabove. The only amendments made thereto pertain to minor formal matters. Namely, the expression "conduction type" in dependent claim 3 was revised to the more prevalent expression "conductivity type". Also, with regard to dependent claim 8, the expression "a second single crystal layer", in lines 2-3 thereof, was amended to read instead as the

second single crystal layer, noting that the referred to "second single crystal layer" was appropriately set forth with regard to base independent claim 7 thereof. In view of the amendment to claim 8, the outstanding objection thereto, it is submitted, has been rendered moot.

Discussion will now turn to Items 2-3 of the outstanding Office Action and with regard to the amendments made to Figs 13-15 of the drawings.

The invention according to claim 5 and 7 is intended to cover semiconductor device schemes such as that illustrated in connection with Figs. 13, 14 and 15, although not limited thereto. Fig. 13 shows a cross-sectional view of a main portion of a field effect transistor described in connection with embodiment 4, beginning on page 54 of the present Specification. The Fig. 14 cross-sectional view is illustrative of a main portion of a field effect semiconductor device according to disclosed embodiment 5, described beginning on page 63 of the Specification, and the embodiment shown with regard to the cross-sectional view in Fig. 15 of the drawings relates to a main portion of another field effect semiconductor device in connection with a further aspect of embodiment 5. In each of these illustrations, the field effect semiconductor device is formed in an opening of an insulating film. The opening in the insulating film is an indispensable part or element (or structural characteristic) of the present invention. Supportive showing of this is given below. The following discussion will also show a clear supportive basis in the description in connection with the amendments to Figs. 13, 14 and 15 of the drawings.

In support of the addition of the insulating film 2 in connection with Figs. 13, 14 and 15, the following is an example of supportive discussion directed thereto in the Specification:

(i) It is stated on page 55, lines 3-5, "The basic cross-sectional structure of the field effect semiconductor device in this embodiment is as shown schematically in Fig. 1." As can be seen from the Fig. 1 illustration, the first and second crystal layers 3 and 4 are formed in an opening 6 that is formed in the insulating film 2. This is specifically noted on page 55, lines 7-9, of the Specification.

(ii) On page 58, lines 20-22, of the Specification, related to Embodiment 4, the following is stated: "Since the method of forming the SiC layer or (SiGe)C layer locally on the Si substrate is described separately, this is omitted in this chapter." This relates to the field effect semiconductor device described with regard to Fig. 13 of the drawings. However, as noted above, the basic cross-sectional structure of such an FET semiconductor device has been shown to require the construction thereof in an opening in an insulating film such as insulating film 2, in like manner as that shown in Fig. 1 of the drawings. Therefore, the changes effected in Fig. 13 of the drawings, with regard to the replacement drawing sheet, can be said to be fully supported by the original disclosure.

(iii) With regard to Fig. 14 of the drawings, which is discussed in Embodiment 5 in the Specification, an SOI substrate 200 having also an Si layer 81 and a buried insulating film layer 91 is used for the substrate, in place of the Si substrate 81 of Fig. 13. On page 63, lines 20-22, the inventors state that "the manufacturing steps [of the Embodiment 5] are substantially the same as those in Embodiment 4," except that in Embodiment 5, such as it relates to Fig. 14 of the drawings, the construction is associated with an SOI substrate. In Fig. 14 an SiC layer 83 and an (SiGe)C layer 82 are formed on the substrate in the same manner as that with regard to Embodiment 4 (Fig. 13). That is except for the formation of the SOI substrate, the remaining steps with regard to Fig. 14 are similar as that for Fig. 13. Fig. 15 is another example related to Embodiment 5. Herein, the step of implanting B impurities of the Si layer is not necessary. The other steps in the manufacture thereof, however, are similar to that of Embodiment 4.

> In other words, clear support exists in the Specification for the formation of the semiconductor layers in an opening of an insulating film similarly to that of opening 6 in the Fig. 1 illustration.

It can therefore be said that clear antecedent support is found in the original disclosure with regard to the present changes implemented in Figs. 13, 14 and 15, as depicted in the Replacement Drawing Sheet 12/16. Accordingly, acceptance and formal entry of the Replacement Sheet for original drawing sheet 12/16 is respectfully requested.

Applicants note with appreciation the indication that claims 1-6 and 10-17 are allowable and, moreover, also appreciate the indication that the subject matter of claims 8 and 9 are also considered allowable and that these claims would be formally allowed upon being re-presented in an appropriate self-contained format and upon obviating the outstanding drawing objections/claim objections related thereto. It is submitted, in view of the amendments made to the drawings as well as with regard to claim 8 and as supplemented with the above discussion, any and all previously rendered concerns have been overcome. Therefore, insofar as presently applicable, the outstanding objections to the drawings/claim 8 are traversed and withdrawal of the same is respectfully requested.

Discussion will now turn to the outstanding art rejection. As will be shown below, the invention according to independent claim 7 was neither disclosed or suggested from Notsu et al. (U.S. Patent No. 2002/0146892 A1). Therefore, insofar as presently applicable, the rejection of claim 7 under 35 USC §102(e) and, alternatively, under 35 USC §103(a), are traversed and reconsideration and withdrawal of the same are respectfully requested.

It is stated in the rejection that:

> "The '892 reference discloses in the figures, particularly Figs. 3A and 5C, and respective portions of the Specification a semiconductor device, the device having the characteristics as claimed and as interpreted for the first and second single crystal layers in the embodiment of Fig. 3A and the characteristics as claimed and as interpreted for the gate/channel/source/drain device (a transistor as is known in the art) in the Embodiment of Fig. 5C. The reference further teaches in paragraph [0188] that the Embodiment of Fig. 5C is applicable to the embodiment of Fig. 3A." (See the paragraph bridging pages 4-5 of the Official Action.)

A careful review of Natsu et al. (Reference '892) shows that the layer 1105 which is used in the circuit element such as that shown in Figs. 5A, 5B, 5C and 5D is a strained Si layer like atrained Si layer141 with regard to Fig. 3F of Natsu et al. This is clearly evident from the supportive discussion in paragraphs [0179], [0180] and [0188] of Natsu et al. For example, in the discussion in paragraph [0188], lines 4-6 thereof, the following is stated:

> "As described above, this semiconductor substrate has an SiGe layer on the buried oxide film (insulating film) and a strained Si layer on it."

The SiGe layer 1006 in Fig. 5C of Natsu et al., it is submitted, corresponds to a layer 114 in Fig. 3F, and the strained Si layer 1105 thereof corresponds to the strained Si layer 141 (in Fig. 3F). Consistent with that stated in paragraphs [0130], [0170] and [0171], with regard to the Fig. 3A showings in Natsu et al., both of the single crystalline Si layers 113 and 115 are not strained and a single crystalline Si layer 114 is a strained layer. In connection with this, also, the following is noted with regard to paragraph [0171] in Natsu et al.:

> "Next to the step shown in Fig. 3A, in the step

(insulating layer forming step/first diffusion) shown in Fig. 3B, an insulating layer 121 is formed on the surface of the first substrate 110 shown in Fig 3 A by thermal oxidation."

The single crystalline silicon layer 115, it is noted, is changed into an insulating layer 121 such as shown in Fig. 3B.

According to the discussion in paragraphs [0177] and [0178] in Natsu et al., annealing makes a single crystalline Si layer into a SiGe layer 114 in which, also, germanium is diffused into the silicon layer 113. In the case of Figs. 3F and 5C, forming of the SiGe layers 114" and 1006 is used in order to cause the strain to the strained Si layer 141 and 1105 and, it is submitted, it is not used to obtain good crystallinity (Quality of crystallinity) of the strained Si layers 141 and 1105 in Figs 3F and 5, respectively. Therefore, the multi-layer 1006/1105 shown in Fig. 5C in Natsu et al., Applicants submit, is quite different from the single crystalline multi-layer construction of multi-layer 82/83 shown in Figs. 13,14 and 15 of the present application, which are example illustrations thereof of the invention such as that set forth in claim 7.

As noted from the discussion in paragraph [0189] of Natsu et al., the element isolation region (insulating layer) 1054, in Fig. 5A, is formed by manufacturing a SOI substrate having a multi-layer 1006/1005 construction. However, a very important physical characteristic according to the present invention is that a single crystalline multi-layer scheme is provided inside of an opening formed in an insulating layer, an example of which is shown in connection with multi-layer 82/83 structure, formed in an opening of insulating film 2, shown with regard to Figs. 13, 14 and 15, although not limited thereto. The formation of a single crystalline layer on only a local region

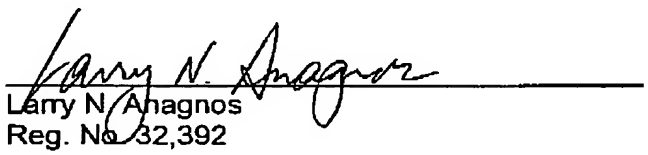
such as that effected in accordance with the present invention leads to very high quality crystallinity. Therefore, for at least the above reasons, the invention according to claim 7 could not have been anticipated or, for that matter, rendered obvious such as alleged in the outstanding alternative rejection.

Therefore, in view of the amendments presented hereinabove together with these accompanying remarks, reconsideration and withdrawal of the outstanding objections/rejection as well as favorable action on all of the currently pending claims, i.e., claims I-17, and an early formal notification of allowance of the present application is respectfully requested.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (Docket No. 520.43558X00), and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



Larry N. Anagnos
Reg. No. 32,392

LNA/gjb
703-312-6600